IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P012

Inventor(s): Linus Torvalds, Robert Bedichek and Stephen Johnson

Group Art Unit: 2183

Filed: 10/13/99

Examiner: Ellis, Richard L.

Application No.: 09/417,980

Title: A METHOD FOR TRANSLATING INSTRUCTIONS IN A SPECULATIVE MICROPROCESSOR FEATURING COMMITTING STATE (AS AMENDED)

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following documents:

Author, Title, Date, Place (e.g. Journal) of Publication

Wen-Mei W. Hwa and Yale N. Patt, CHECKPOINT REPAIR FOR OUT-OF-ORDER EXECUTION MACHINES, 1987, Proceedings of the 14th Annual International Symposium on Computer Architecture

Alberto Ferreira De Souza and Peter Rounce, DYNAMICALLY SCHEDULING THE TRACE PRODUCED DURING PROGRAM EXECUTION INTO VLIW INSTRUCTIONS, 04/12/99, Proceedings of the 13th International Parallel Processing Symposium 10th Symposium on Parallel and Distributed Programming

Alberto Ferreira De Souza, Home Page, retrieved 01/20/05, http://www.inf.ufes.br/alberto/papers/desouza_rounce99a.pdf)>

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Respectfully submitted,

Date: 3/18/05

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Attorney Docket No.: TRAN-P012

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	L							
	M							
	N							
	O							
	P							
	Q							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	Wen-Mei W. Hwa and Yale N. Patt, CHECKPOINT REPAIR FOR OUT-OF-ORDER EXECUTION MACHINES, 1987, Proceedings of the 14th Annual International Symposium on Computer Architecture
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Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.